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Claims

[c1] 1. A method for predicting manufacturing yield for a proposed integrated circuit, comprising in the order recited:

(a) providing a multiplicity of different integrated circuit library elements in a design database, each library element linked to a corresponding normalization factor in said design database;

(b) selecting library elements from said design database to include in a proposed design for said integrated circuit;

(c) generating an equivalent circuit count of said proposed design based on said normalization factors and a count of each different library element included in said proposed design; and

(d) calculating a predicted manufacturing yield based on said equivalent circuit count, a predicted density of manufacturing defects and an area of said proposed integrated circuit chip.

[c2] 2. The method of claim 1 wherein step (c) includes multiplying each count of each different library element included in said proposed design by said corresponding

normalization factors to obtain a set of normalized circuit counts by said different design elements and summing said set of normalized circuit counts to obtain said equivalent circuit count for said proposed design.

[c3] 3. The method of claim 1, further including after step (d):

(e) determining if said predicted manufacturing yield for said proposed design meets predetermined criteria; and if said predicted manufacturing yield does not meet said predetermined criteria, changing one or more design elements or design element counts and repeating steps (b) through (e).

[c4] 4. The method of claim 1, further including after step (d):

generating a completed design for said integrated circuit;

performing a critical area yield analysis to determine a critical area analysis yield of said completed design;

comparing said critical area analysis yield to said predicted manufacturing yield; and

based on said comparison, changing normalization factors for selected library elements in said design database.

[c5] 5.The method of claim 1, further including:

manufacturing said integrated circuit;
analyzing the yield of said integrated circuit;
based on said analysis of yield of said integrated circuit, changing said normalization factors for selected library elements in said design database.

[c6] 6. The method of claim 1, wherein said library elements are linked to said normalization factors by assigning each different library element of said design database to one of a multiplicity of circuit types and assigning said normalization factors to said circuit types.

[c7] 7. The method of claim 6, further including after step (d):
generating a completed design for said integrated circuit;
performing a critical area yield analysis of said completed design;
comparing said critical area yield analysis to said predicted manufacturing yield; and
based on said comparison, changing the circuit type of selected design elements or changing the normalization factor for selected circuit types of said multiplicity of circuit types.

[c8] 8. The method of claim 6, further including
manufacturing said integrated circuit;

analyzing the yield of said integrated circuit;
based on said analysis of yield of said integrated circuit, changing the circuit type of selected design elements or changing the normalization factor for selected circuit types of said multiplicity of circuit types.

[c9] 9. The method of claim 1, wherein said normalization factors are based on analysis of the effect of a multiplicity of different circuit types on manufacturing yield of a multiplicity of different integrated circuits.

[c10] 10. The method of claim 1, wherein said normalization factors normalize memory library elements by bit count and logic library elements by circuit count.

[c11] 11. The method of claim 1, wherein said defect density value is a function of technology
and time.

[c12] 12. A method for predicting manufacturing yield for an integrated circuit, comprising in the order recited:
(a) assigning different integrated circuit library elements into circuit types according to a user defined list of attributes;
(b) compiling a set of yield limiting parameters for each circuit type and determining a normalization factor for each circuit type;

(c) selecting library elements from said design database to include in a proposed design for said integrated circuit;

(d) generating an equivalent circuit count of said proposed design based on said normalization factors for said circuit types and a count of each different library element included in said proposed design; and

(e) calculating a predicted manufacturing yield based on said equivalent circuit count, a defect density value and an area of said proposed integrated circuit chip.

[c13] 13. The method of claim 12 wherein step (d) includes multiplying each count of each different library element included in said proposed design by said corresponding normalization factors for said circuit type that each design element is assigned to in order to obtain a set of normalized circuit counts by said different design elements and summing said set of normalized circuit counts to obtain said equivalent circuit count for said proposed design.

[c14] 14. The method of claim 12, further including after step (e):

(f) determining if said predicted manufacturing yield for said proposed design meets predetermined criteria; and if said predicted manufacturing yield does not meet said predetermined criteria, changing one or more design el-

ements or design element counts and repeating steps (c) through (f).

[c15] 15. The method of claim 12, further including after step (e):
generating a completed design for said integrated circuit;
performing a critical area yield analysis to determine a critical area analysis yield of said completed design;
comparing said critical area analysis yield to said predicted manufacturing yield; and
based on said comparison, changing the circuit type of selected design elements or changing the normalization factor for selected circuit types of said multiplicity of circuit types.

[c16] 16. The method of claim 12, further including
manufacturing said integrated circuit;
analyzing the yield of said integrated circuit;
based on said analysis of yield of said integrated circuit, changing the circuit type of selected design elements or changing the normalization factor for selected circuit types of said multiplicity of circuit types.

[c17] 17. The method of claim 12, wherein said normalization factors are based on analysis of the effect of a multiplicity of different circuit types on manufacturing yield of a

multiplicity of different integrated circuits.

[c18] 18. The method of claim 12, wherein said normalization factors normalize memory library elements by bit count and logic library elements by circuit count.

[c19] 19. The method of claim 12, wherein said defect density value is a function of technology and time.

[c20] 20. The method of claim 12, wherein said attributes include one or more of a memory or logic tag, analog or digital tag, circuit function, circuit complexity, number and type of masking levels, number of devices, redundancy and shape density for each library element.

[c21] 21. A computer system comprising a processor, an address/data bus coupled to said processor, and a computer-readable memory unit adapted to be coupled to said processor, said memory unit containing instructions that when executed by said processor implement a method for predicting manufacturing yield for an integrated circuit, said method comprising the computer implemented steps of:

(a) providing a multiplicity of different integrated circuit library elements in a design database, each library element linked to a corresponding normalization factor in said design database;

(b) selecting library elements from said design database to include in a proposed design for said integrated circuit;

(c) generating an equivalent circuit count of said proposed design based on said normalization factors and a count of each different library element included in said proposed design; and

(d) calculating a predicted manufacturing yield based on said equivalent circuit count, a predicted density of manufacturing defects and an area of said proposed integrated circuit chip.

[c22] 22. The system of claim 21 wherein step (c) includes multiplying each count of each different library element included in said proposed design by said corresponding normalization factors to obtain a set of normalized circuit counts by said different design elements and summing said set of normalized circuit counts to obtain said equivalent circuit count for said proposed design.

[c23] 23. The system of claim 21, the method further including after step (d) the steps of:

(e) determining if said predicted manufacturing yield for said proposed design meets predetermined criteria; and if said predicted manufacturing yield does not meet said predetermined criteria, changing one or more design elements or design element counts and repeating steps (b)

through (e).

[c24] 24. The system of claim 21, the method further including after step (d) the steps of:
generating a completed design for said integrated circuit;
performing a critical area yield analysis to determine a critical area analysis yield of said completed design;
comparing said critical area analysis yield to said predicted manufacturing yield; and
based on said comparison, changing normalization factors for selected library elements in said design database.

[c25] 25.The system of claim 21, the method further including:
manufacturing said integrated circuit;
analyzing the yield of said integrated circuit;
based on said analysis of yield of said integrated circuit, changing said normalization factors for selected library elements in said design database.

[c26] 26. The system of claim 21, wherein said library elements are linked to said normalization factors by assigning each different library element of said design database to one of a multiplicity of circuit types and assigning said normalization factors to said circuit types.

[c27] 27. The system of claim 26, the method further including after step (d) the steps of:
generating a completed design for said integrated circuit;
performing a critical area yield analysis of said completed design;
comparing said critical area yield analysis to said predicted manufacturing yield; and
based on said comparison, changing the circuit type of selected design elements or changing the normalization factor for selected circuit types of said multiplicity of circuit types.

[c28] 28. The system of claim 26, the method further including the steps of:
manufacturing said integrated circuit;
analyzing the yield of said integrated circuit;
based on said analysis of yield of said integrated circuit, changing the circuit type of selected design elements or changing the normalization factor for selected circuit types of said multiplicity of circuit types.

[c29] 29. The system of claim 21, wherein said normalization factors are based on analysis of the effect of a multiplicity of different circuit types on manufacturing yield of a multiplicity of different integrated circuits.

[c30] 30. The system of claim 21, wherein said normalization factors normalize memory library elements by bit count and logic library elements by circuit count.

[c31] 31. The system of claim 21, wherein said defect density value is a function of technology and time.